DDR4 Datasheet

RS512M16Z2DD-62DT

96-Ball

Revision 1.2

July. 18. 2024

Revision History

Version	Date	Editor
V1.0	2023-4-27	Basic spec and architecture
V1.1	2024-04-24	Add a new package size
V1.2	2024-07-18	Add a new package size

Notes： *This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change at any time without notice, as further product development and data characterization sometimes occur.*

Contents

1. Product Overview

1.1. Feature Overview

- V_{DD} = V_{DDQ} = 1.2V ±60mV
- V_{PP} = 2.5V, –125mV/+250mV
- On-die, internal, adjustable VREFDQ generation
- 1.2V pseudo open-drain I/O
- TC of 0°C to 95°C
  - 64ms, 8192-cycle refresh at 0°C to 85°C
  - 32ms at 85°C to 95°C
- TC of 0°C to 95°C
- 8 internal banks (x16): 2 groups of 4 banks each
- 8n-bit prefetch architecture
- Programmable data strobe preambles
- Data strobe preamble training
- Command/Address latency (CAL)
- Multipurpose register READ and WRITE capability
- Write and read leveling
- Self refresh mode
- Low-power auto self refresh (LPASR)
- Temperature controlled refresh (TCR)
- Fine granularity refresh
- Self refresh abort
- Maximum power saving
- Output driver calibration
- Nominal, park, and dynamic on-die termination (ODT)
- Data bus inversion (DBI) for data bus
- Command/Address (CA) parity
- Databus write cyclic redundancy check (CRC)
- Per-DRAM addressability
- Connectivity test (x16)
- Post package repair (PPR) and soft post package repair (sPPR) modes
- JEDEC JESD-79-4 compliant
- Rayson Memory
- Array configuration
  - 512Meg x 16
- Product Code

- DDR4
- Density
  - 8Gigabyte
- Voltage/Refresh
  - 1.2V/8K refresh
- FBGA package (Pb-free) - x16
  - 96-ball (7.5mm x 13mm x 1.2mm Max)
  - 96-ball (7.5mm x 13.5mm x 1.2mm Max)
- Timing - cycle time
  - 0.625ns @ CL = 22 (DDR4-3200)
- Operating Temperature
  - Commercial (0°≤TC ≤95°C)

2. Physical Specification

2.1. Package ballout & Addressing

96-Ball FBGA – x16 Ball Assignments

	1	2	3	4	5	6	7	8	9	
A	VDDQ	VSSQ	DQU0				DQSU_c	VSSQ	VDDQ	A
B	VPP	VSS	VDD				DQSU_t	DQU1	VDD	B
C	VDDQ	DQU4	DQU2				DQU3	DQU5	VSSQ	C
D	VDD	VSSQ	DQU6				DQU7	VSSQ	VDDQ	D
E	VSS	DMU_n DBIU_n	VSSQ				DML_n DBIL_n	VSSQ	VSS	E
F	VSSQ	VDDQ	DQSL_c				DQL1	VDDQ	ZQ	F
G	VDDQ	DQL0	DQSL_t				VDD	VSS	VDDQ	G
H	VSSQ	DQL4	DQL2				DQL3	DQL5	VSSQ	H
J	VDD	VDDQ	DQL6				DQL7	VDDQ	VDD	J
K	VSS	CKE	ODT				CK_t	CK_c	VSS	K
L	VDD	WE_n/ A14	ACT_n				CS_n	RAS_n A16	VDD	L
M	VREFCA	BG0	A10/AP				A12/ BC_n	CAS_n A15	VSS	M
N	VSS	BA0	A4				A3	BA1	TEN	N
P	RESET_n	A6	A0				A1	A5	ALERT_n	P
R	VDD	A8	A2				A9	A7	VPP	R
T	VSS	A11	PAR				NC	A13	VDD	T

2.2. Pad Definition

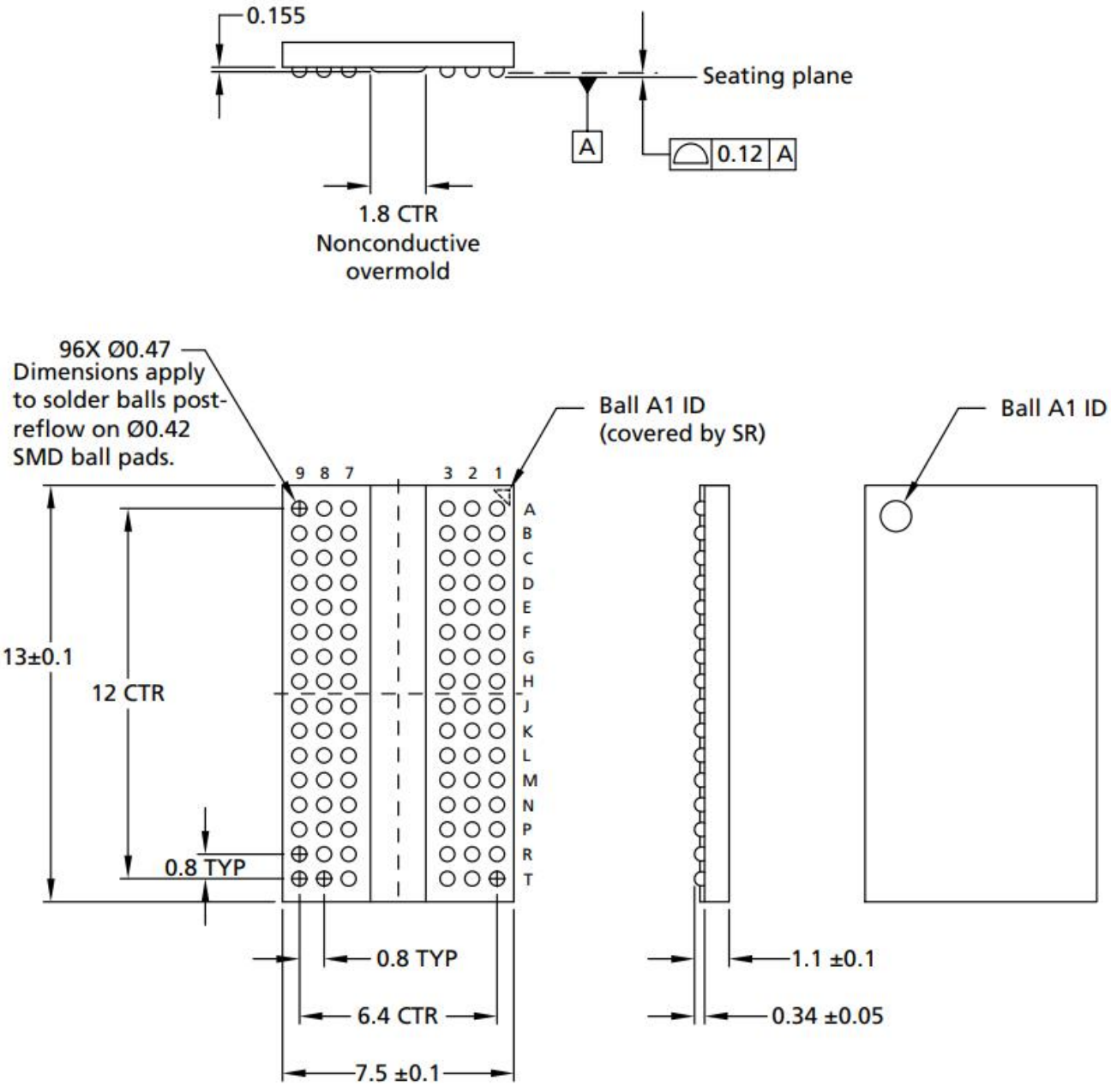
Symbol	Type	Description
A[16:0]	Input	**Address Inputs:** Provide the row address for ACTIVATE commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see coresponding en- tries in this table. The address inputs also provide the op-code during Mode Register Set commands.
A10/AP	Input	**Auto-precharge:** A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (High: Autoprecharge; Low: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 Low) or all banks (A10 High). If only one bank is to be precharged, the bank is selected by bank addresses.
A12/BC_n	Input	**Burst Chop:** A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (High, no burst chop; Low: burst chopped). See “Command Truth Table” of Operation Guide for details.
RESET_n	Input	**Active Low Asynchronous Reset:** Reset is active when RESET_n is Low, and inactive when RESET_n is High. RESET_n must be High during normal op- eration. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD
DQ	Input /Output	**Data Input/ Output:** Bi-directional data bus. If CRC is enabled via mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. During this mode, RTT value should be set to Hi-Z. Refer to vendor specific data sheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t,DQSU_c, DQSL_t,DQSL_c	Input /Output	**Data Strobe:** output with Read data, input with Write data.Edge-aligned with Read data, centered-aligned with Write data. For the x16, DQSL corresponds to the data on DQL0-DQL7;DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential sig- nals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during Reads andWrites. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
BG[1:0]	Input	**Bank Group Inputs:** BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. x4/x8 have BG0 and BG1, but x16 has only BG0
BA[1:0]	Input	**Bank Address Inputs:** BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.

Symbol	Type	Description
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c power-down. Input buffers (excluding CKE and RESET_n) are disabled during self refresh.
CKE	Input	**Clock Enable:** CKE High activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power- Down and Self-Refresh operation (all banks idle), or Ac- tive Power-Down (row Active in any bank). CKE is synchronous for Self-Re- fresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all op- erations (including Self-Refresh). CKE must be maintained high throughout Read and Write accesses. Input buffers, excluding CK_t,CK_c, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh
CS_n	Input	**Chip Select:** All commands are masked when CS_n is registered High. CS_ n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code
ODT	Input	**On Die Termination:** ODT (registered High) enables R_{TT}_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configura- tions. For x16 configuration ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable R_{TT}_NOM
ACT_n	Input	**Activation Command Input:** ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/ A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	**Command Inputs:** RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For ex- ample, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are command pins for Read, Write and other commands defined in Command Truth Table
DM_n/DBI_n, TDQS_t, (DMU_n/DBIU_n) (DML_n/ DBIL_n)	Input/Output	**Input Data Mask and Data Bus Inversion:** DM_n is an input mask signal for Write data. Input data is masked when DM_n is sampled Low coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10, A11, A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Reg- ister A11 setting in MR1. DBI_n is an input/output identifying whether to store/ output the true or inverted data. If DBI_n is Low, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is High. TDQS is only supported in X8

Symbol	Type	Description
TDQS_t, TDQS_c	Output	**Termination Data Strobe:** TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11 = 0 in MR1, DM/DBI/ TDQS will provide the data mask function or Data Bus Inversion depending on MR5; A11, A12, A10 and TDQS_c is not used. x4/ x16 DRAMs must dis- able the TDQS function via mode register A11 = 0 in MR1.
PAR	Input	**Command and Address Parity Input:** DDR4 Supports Even Parity Check in DRAMs with MR setting. Once it is enabled via Register in MR5, then DRAM calculates Parity with ACT_n,RAS_n/A16,CAS_n/A15,WE_n/A14,BG0-BG1,BA0-BA1,A17-A0.Input parity should maintain at the rising edge of the clock and at the same time with command & address with CS_n Low
ALERT_n	Input/Output	**ALERT:** It has multi functions such as CRC error flag, Command and Address Parity error flag as output signal. If there is error in CRC, then Alert_n goes Low for the period time interval and goes back High. If there is error in Command Address Parity Check, then ALERT_n goes Low for relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as an input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n pin must be bounded to VDD on board.
TEN	Input	**Connectivity Test Mode Enable:** Required on X16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb.High in this pin will en- able Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on system. This pin may be DRAM internally pulled Low through a weak pull-down resistor to VSS.
NC		**No Connect:** No internal electrical connection is present.
VDDQ	Supply	**DQ Power Supply:** 1.2 V +/- 0.06 V
VSSQ	Supply	**DQ Ground**
VDD	Supply	**Power Supply:** 1.2 V +/- 0.06 V
VSS	Supply	**Ground**
VPP	Supply	**DRAM Activating Power Supply:** 2.5V (2.375V min, 2.75V max)
VREFCA	Supply	**Reference voltage for CA**
ZQ	Supply	**Reference Pin for ZQ calibration**

2.3. Discrete Package Dimension

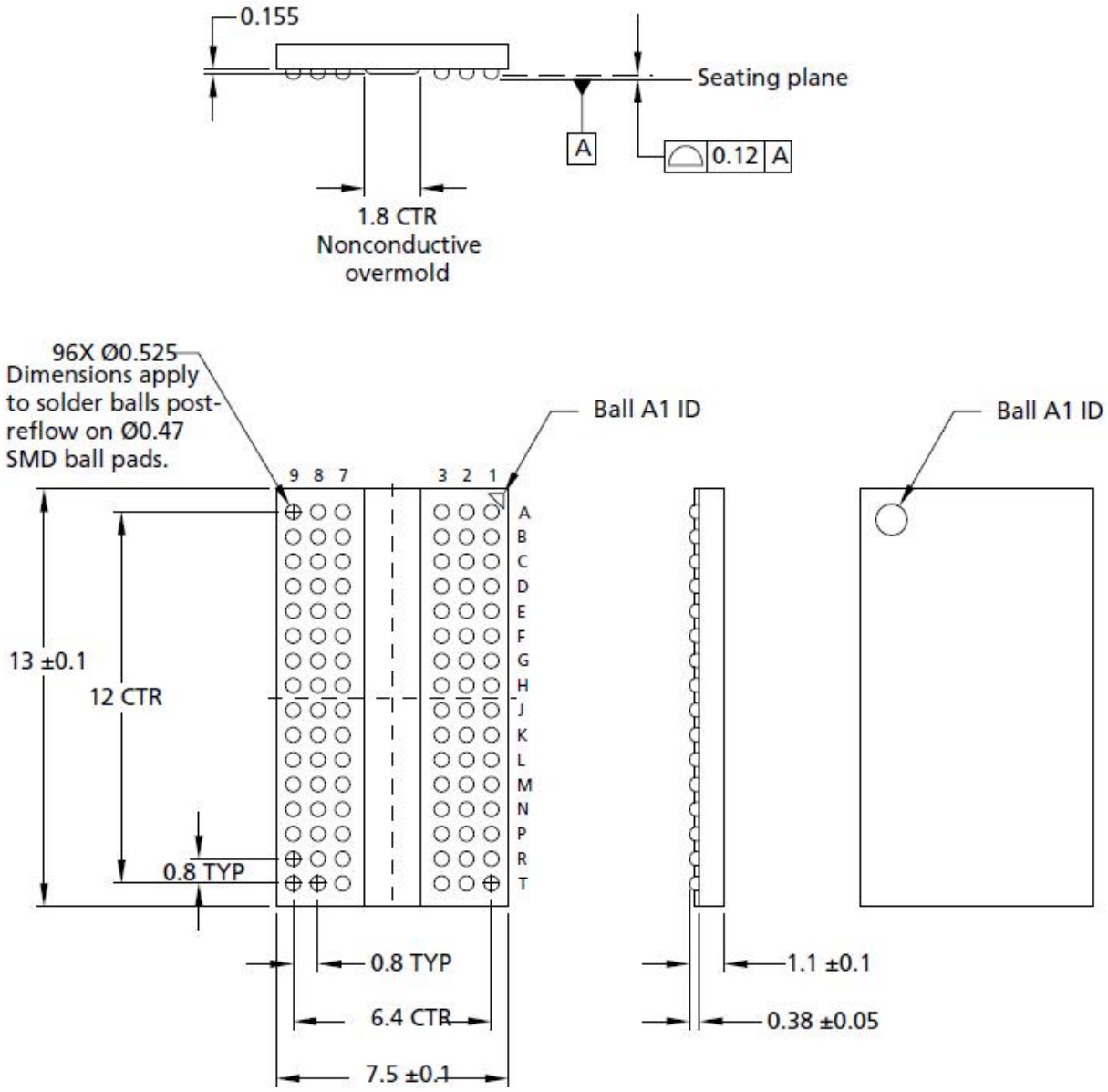
7.5mm X13mm (Package A)



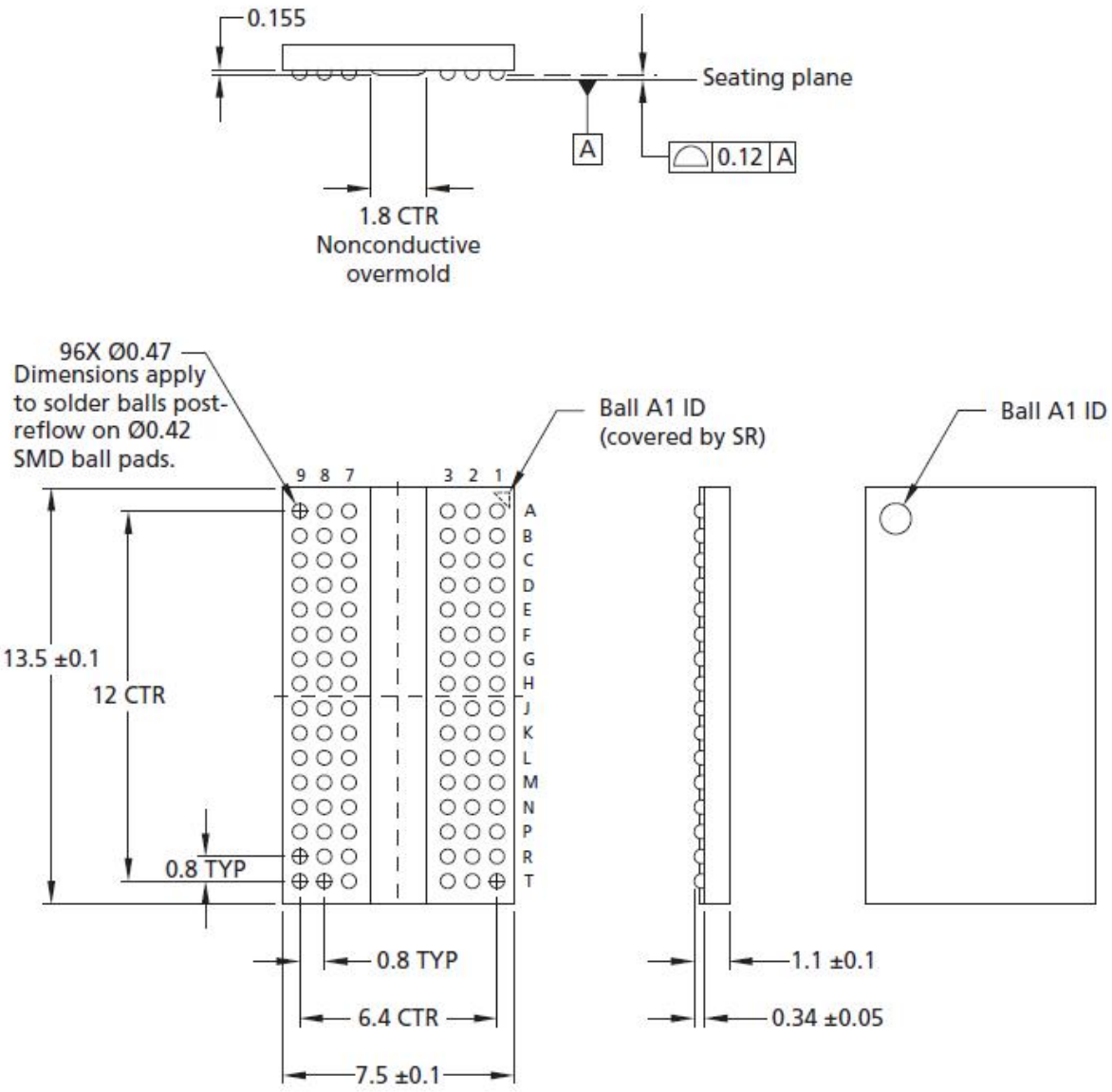
Notes: 1、All dimensions are in millimeters.

2、Solder ball material: SAC302 (Pb-free 96.5% Sn, 3% Ag, 0.2% Cu)

7.5mm X13mm (Package B)

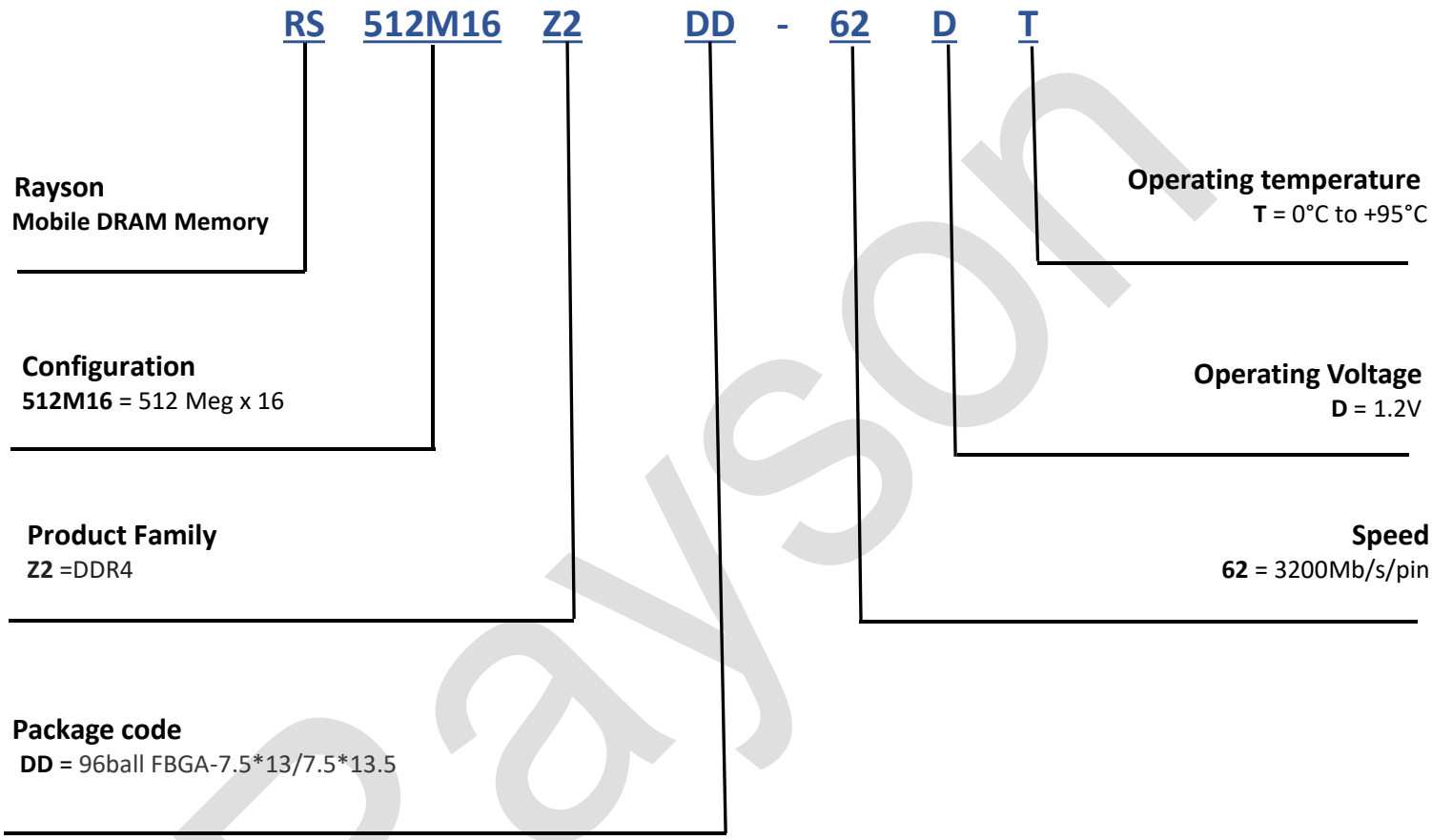


7.5mm X13.5mm (PackageC)



3. Core Specifications

3.1. Part Number Decoding



3.2. Ordering Options

Table 1: Key Timing Parameters

Speed	DDR4-3200	Unit
	22-22-22	
tCK (min)	0.625	ns
CAS Latency	22	nCK
tRCD (min)	13.75	ns
tRP (min)	13.75	ns
tRAS (min)	32	ns
tRC (min)	45.75	ns

Table 2: Part Number List

Part Number	Organization	Data Rate	CL-^{t}RCD-^{t}RP
RS512M16Z2DD-62DT	512Mb x 16	3200 Mb/s/pin	22-22-22

3.3. Die Addressing Table

Parameter	512 Meg × 16
Number of Bank Groups	2
Bank Group Address	BG0
Bank count per group	4
Bank Address per Bank Group	BA[1:0]
Row Address	64K (A[15:0])
Column Address	1K (A[9:0])
Page Size	2KB

Notes: 1、Page size is per bank, calculated as follows:
Page size = 2COLBITS x ORG/8, where COLBIT = the number of column address bits and ORG = the number of DQ bits.
2、Die revision dependent.