



# Industrial LPDDR4/4X Datasheet

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**ATL4X2G32M1D-46IT**

**ATL4X4G32M1D-46IT**

**200-ball FBGA**

**Revision 1.0**

**Apr. 18. 2023**

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## Revision History

| Version | Date      | Editor | Remark                      |
|---------|-----------|--------|-----------------------------|
| V1.0    | 2023-4-18 | eddy   | Basic spec and architecture |

**Notes:** This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change at any time without notice, as further product development and data characterization sometimes occur.



# Contents

|                                              |    |
|----------------------------------------------|----|
| 1. Product Overview .....                    | 4  |
| 2. Physical Specifications .....             | 5  |
| 2.1. Package Block Diagrams .....            | 5  |
| 2.2. Ball Assignments and Descriptions ..... | 7  |
| 2.3. Pad Definition .....                    | 9  |
| 2.4. Discrete Package Dimension .....        | 11 |
| 3. Core Specifications .....                 | 11 |
| 3.1. Part Number Decoding .....              | 12 |
| 3.2. Ordering Options .....                  | 13 |
| 3.3. Die Addressing Table .....              | 14 |
| 3.4. Mode Register Contents .....            | 15 |



# 1. Product Overview

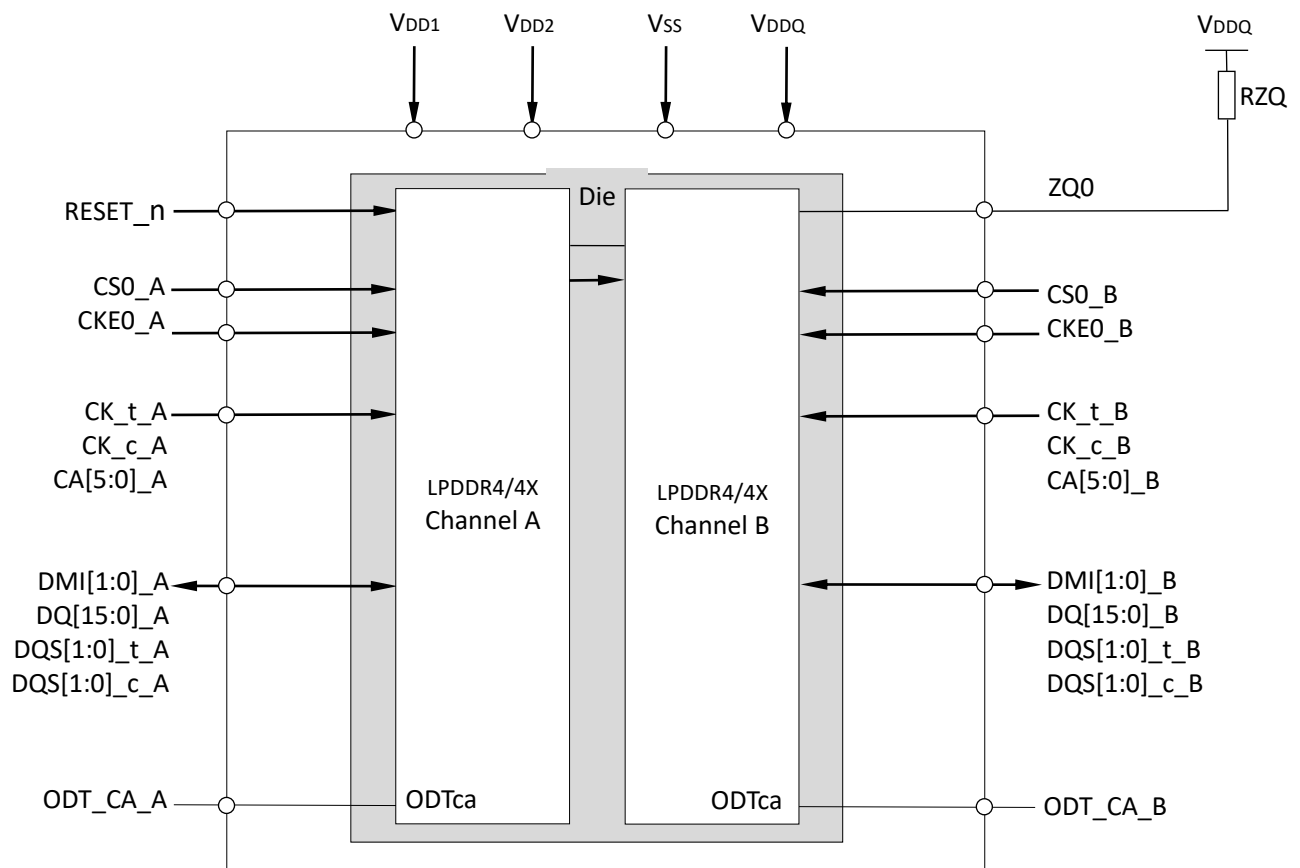
- Ultra-low-voltage core and I/O power supplies
  - $V_{DD1}$  = 1.70-1.95V; 1.80V nominal
  - $V_{DD2}$  = 1.06-1.17V; 1.10V nominal
  - $V_{DDQ}$  = 0.57-0.65V; 0.60V nominal Or  $V_{DDQ}$  = 1.06-1.17V; 1.10V nominal
- Frequency range
  - 2133-10 MHz (data rate range per pin:4266-20Mbps)
- 16n prefetch DDR architecture
- 8 internal banks per channel for concurrent operation
- Single-data-rate CMD / ADR entry
- Bidirectional / differential data strobe per byte lane
- Programmable READ and WRITE latencies (RL / WL)
- Programmable and on-the-fly burst lengths (BL = 16, 32)
- Directed per-bank refresh for concurrent bank operation and ease of command scheduling
- Up to 8.53 GB / s per die x16 channel
- On-chip temperature sensor to control self refresh rate
- Partial-array self refresh (PASR)
- Selectable output drive strength (DS)
- Clock-stop capability
- RoHS-compliant, “green” packaging
- Programmable  $V_{SS}$  (ODT) termination
- Single-ended CK and DQS support
- Array configuration
  - 2GB: 512 Meg x 32 (2 channels x 16 I/O)
  - 4GB: 1 Gig x 32 (2 channels x 16 I/O)
- Device configuration
  - 2GB: 512M32 x 1 die in package
  - 4GB: 512M32 x 2 die in package
- “green” package
  - 200-ball FBGA (10mm x 14.5mm x Seated height 1.1mm Max)
- Speed grade,cycle time
  - 468ps@ RL = 36/40

- Temperature range
  - Operating temperature range : -40°C to + 95°C
  - Storage temperature range : -55°C to + 125°C

## 2. Physical Specifications

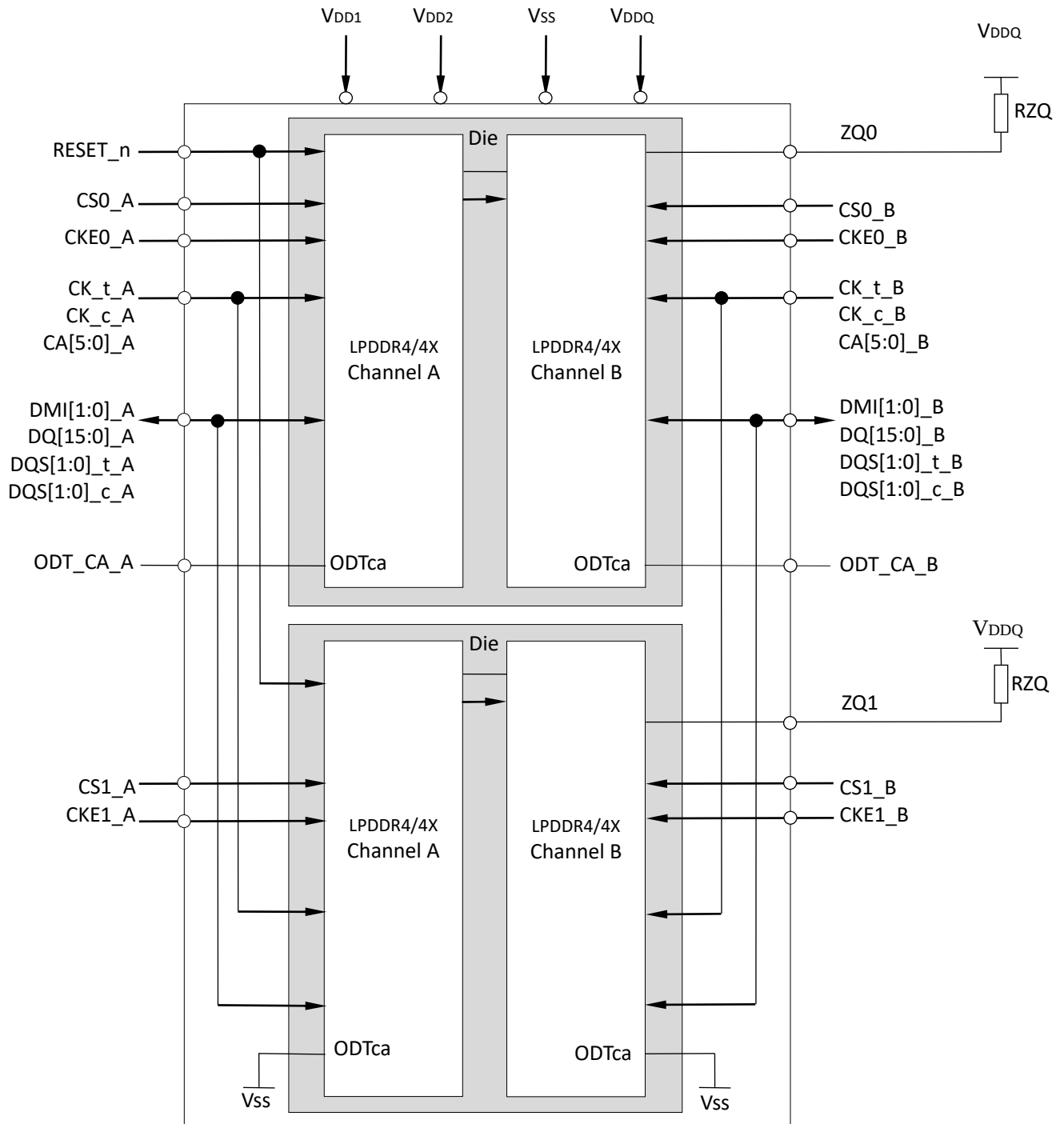
### 2.1. Package Block Diagrams

Single-Die, Dual-Channel, Single-Rank Package Block Diagram



### Package Block Diagrams (continue)

Dual-Die, Dual-Channel, Dual-Rank Package Block Diagram





## 2.2. Ball Assignments and Descriptions

### 200-Ball Single-Die, Dual-Channel, Single-Rank Discrete FBGA

|    | 1                | 2               | 3                | 4                | 5                | 6 | 7 | 8                | 9                | 10               | 11              | 12               |
|----|------------------|-----------------|------------------|------------------|------------------|---|---|------------------|------------------|------------------|-----------------|------------------|
| A  | DNU              | DNU             | V <sub>SS</sub>  | V <sub>DD2</sub> | ZQ0              |   |   | NC               | V <sub>DD2</sub> | V <sub>SS</sub>  | DNU             | DNU              |
| B  | DNU              | DQ0_A           | V <sub>DDQ</sub> | DQ7_A            | V <sub>DDQ</sub> |   |   | V <sub>DDQ</sub> | DQ15_A           | V <sub>DDQ</sub> | DQ8_A           | DNU              |
| C  | V <sub>SS</sub>  | DQ1_A           | DMI0_A           | DQ6_A            | V <sub>SS</sub>  |   |   | V <sub>SS</sub>  | DQ14_A           | DMI1_A           | DQ9_A           | V <sub>SS</sub>  |
| D  | V <sub>DDQ</sub> | V <sub>SS</sub> | DQS0_t_A         | V <sub>SS</sub>  | V <sub>DDQ</sub> |   |   | V <sub>DDQ</sub> | V <sub>SS</sub>  | DQS1_t_A         | V <sub>SS</sub> | V <sub>DDQ</sub> |
| E  | V <sub>SS</sub>  | DQ2_A           | DQS0_c_A         | DQ5_A            | V <sub>SS</sub>  |   |   | V <sub>SS</sub>  | DQ13_A           | DQS1_c_A         | DQ10_A          | V <sub>SS</sub>  |
| F  | V <sub>DD1</sub> | DQ3_A           | V <sub>DDQ</sub> | DQ4_A            | V <sub>DD2</sub> |   |   | V <sub>DD2</sub> | DQ12_A           | V <sub>DDQ</sub> | DQ11_A          | V <sub>DD1</sub> |
| G  | V <sub>SS</sub>  | ODT_CA_A        | V <sub>SS</sub>  | V <sub>DD1</sub> | V <sub>SS</sub>  |   |   | V <sub>SS</sub>  | V <sub>DD1</sub> | V <sub>SS</sub>  | NC              | V <sub>SS</sub>  |
| H  | V <sub>DD2</sub> | CA0_A           | NC               | CS0_A            | V <sub>DD2</sub> |   |   | V <sub>DD2</sub> | CA2_A            | CA3_A            | CA4_A           | V <sub>DD2</sub> |
| J  | V <sub>SS</sub>  | CA1_A           | V <sub>SS</sub>  | CKE0_A           | NC               |   |   | CK_t_A           | CK_c_A           | V <sub>SS</sub>  | CA5_A           | V <sub>SS</sub>  |
| K  | V <sub>DD2</sub> | V <sub>SS</sub> | V <sub>DD2</sub> | V <sub>SS</sub>  | NC               |   |   | NC               | V <sub>SS</sub>  | V <sub>DD2</sub> | V <sub>SS</sub> | V <sub>DD2</sub> |
| L  |                  |                 |                  |                  |                  |   |   |                  |                  |                  |                 |                  |
| M  |                  |                 |                  |                  |                  |   |   |                  |                  |                  |                 |                  |
| N  | V <sub>DD2</sub> | V <sub>SS</sub> | V <sub>DD2</sub> | V <sub>SS</sub>  | NC               |   |   | NC               | V <sub>SS</sub>  | V <sub>DD2</sub> | V <sub>SS</sub> | V <sub>DD2</sub> |
| P  | V <sub>SS</sub>  | CA1_B           | V <sub>SS</sub>  | CKE0_B           | NC               |   |   | CK_t_B           | CK_c_B           | V <sub>SS</sub>  | CA5_B           | V <sub>SS</sub>  |
| R  | V <sub>DD2</sub> | CA0_B           | NC               | CS0_B            | V <sub>DD2</sub> |   |   | V <sub>DD2</sub> | CA2_B            | CA3_B            | CA4_B           | V <sub>DD2</sub> |
| T  | V <sub>SS</sub>  | ODT_CA_B        | V <sub>SS</sub>  | V <sub>DD1</sub> | V <sub>SS</sub>  |   |   | V <sub>SS</sub>  | V <sub>DD1</sub> | V <sub>SS</sub>  | RESET_n         | V <sub>SS</sub>  |
| U  | V <sub>DD1</sub> | DQ3_B           | V <sub>DDQ</sub> | DQ4_B            | V <sub>DD2</sub> |   |   | V <sub>DD2</sub> | DQ12_B           | V <sub>DDQ</sub> | DQ11_B          | V <sub>DD1</sub> |
| V  | V <sub>SS</sub>  | DQ2_B           | DQS0_c_B         | DQ5_B            | V <sub>SS</sub>  |   |   | V <sub>SS</sub>  | DQ13_B           | DQS1_c_B         | DQ10_B          | V <sub>SS</sub>  |
| W  | V <sub>DDQ</sub> | V <sub>SS</sub> | DQS0_t_B         | V <sub>SS</sub>  | V <sub>DDQ</sub> |   |   | V <sub>DDQ</sub> | V <sub>SS</sub>  | DQS1_t_B         | V <sub>SS</sub> | V <sub>DDQ</sub> |
| Y  | V <sub>SS</sub>  | DQ1_B           | DMI0_B           | DQ6_B            | V <sub>SS</sub>  |   |   | V <sub>SS</sub>  | DQ14_B           | DMI1_B           | DQ9_B           | V <sub>SS</sub>  |
| AA | DNU              | DQ0_B           | V <sub>DDQ</sub> | DQ7_B            | V <sub>DDQ</sub> |   |   | V <sub>DDQ</sub> | DQ15_B           | V <sub>DDQ</sub> | DQ8_B           | DNU              |
| AB | DNU              | DNU             | V <sub>SS</sub>  | V <sub>DD2</sub> | V <sub>SS</sub>  |   |   | V <sub>SS</sub>  | V <sub>DD2</sub> | V <sub>SS</sub>  | DNU             | DNU              |
|    | 1                | 2               | 3                | 4                | 5                | 6 | 7 | 8                | 9                | 10               | 11              | 12               |

Top View (ball down)

 LPDDR4\_A(Channel A)  LPDDR4\_B(Channel B)  ZQ,ODT\_CA,RESET  Supply  Ground



## Ball Assignments and Descriptions (continue)

### 200-Ball Dual-Die, Dual-Channel, Dual-Rank Discrete FBGA

|    | 1                | 2               | 3                | 4                | 5                | 6 | 7 | 8                | 9                | 10               | 11              | 12               |
|----|------------------|-----------------|------------------|------------------|------------------|---|---|------------------|------------------|------------------|-----------------|------------------|
| A  | DNU              | DNU             | V <sub>SS</sub>  | V <sub>DD2</sub> | ZQ0              |   |   | ZQ1              | V <sub>DD2</sub> | V <sub>SS</sub>  | DNU             | DNU              |
| B  | DNU              | DQ0_A           | V <sub>DDQ</sub> | DQ7_A            | V <sub>DDQ</sub> |   |   | V <sub>DDQ</sub> | DQ15_A           | V <sub>DDQ</sub> | DQ8_A           | DNU              |
| C  | V <sub>SS</sub>  | DQ1_A           | DMI0_A           | DQ6_A            | V <sub>SS</sub>  |   |   | V <sub>SS</sub>  | DQ14_A           | DMI1_A           | DQ9_A           | V <sub>SS</sub>  |
| D  | V <sub>DDQ</sub> | V <sub>SS</sub> | DQS0_t_A         | V <sub>SS</sub>  | V <sub>DDQ</sub> |   |   | V <sub>DDQ</sub> | V <sub>SS</sub>  | DQS1_t_A         | V <sub>SS</sub> | V <sub>DDQ</sub> |
| E  | V <sub>SS</sub>  | DQ2_A           | DQS0_c_A         | DQ5_A            | V <sub>SS</sub>  |   |   | V <sub>SS</sub>  | DQ13_A           | DQS1_c_A         | DQ10_A          | V <sub>SS</sub>  |
| F  | V <sub>DD1</sub> | DQ3_A           | V <sub>DDQ</sub> | DQ4_A            | V <sub>DD2</sub> |   |   | V <sub>DD2</sub> | DQ12_A           | V <sub>DDQ</sub> | DQ11_A          | V <sub>DD1</sub> |
| G  | V <sub>SS</sub>  | ODT_CA_A        | V <sub>SS</sub>  | V <sub>DD1</sub> | V <sub>SS</sub>  |   |   | V <sub>SS</sub>  | V <sub>DD1</sub> | V <sub>SS</sub>  | NC              | V <sub>SS</sub>  |
| H  | V <sub>DD2</sub> | CA0_A           | CS1_A            | CS0_A            | V <sub>DD2</sub> |   |   | V <sub>DD2</sub> | CA2_A            | CA3_A            | CA4_A           | V <sub>DD2</sub> |
| J  | V <sub>SS</sub>  | CA1_A           | V <sub>SS</sub>  | CKE0_A           | CKE1_A           |   |   | CK_t_A           | CK_c_A           | V <sub>SS</sub>  | CA5_A           | V <sub>SS</sub>  |
| K  | V <sub>DD2</sub> | V <sub>SS</sub> | V <sub>DD2</sub> | V <sub>SS</sub>  | NC               |   |   | NC               | V <sub>SS</sub>  | V <sub>DD2</sub> | V <sub>SS</sub> | V <sub>DD2</sub> |
| L  |                  |                 |                  |                  |                  |   |   |                  |                  |                  |                 |                  |
| M  |                  |                 |                  |                  |                  |   |   |                  |                  |                  |                 |                  |
| N  | V <sub>DD2</sub> | V <sub>SS</sub> | V <sub>DD2</sub> | V <sub>SS</sub>  | NC               |   |   | NC               | V <sub>SS</sub>  | V <sub>DD2</sub> | V <sub>SS</sub> | V <sub>DD2</sub> |
| P  | V <sub>SS</sub>  | CA1_B           | V <sub>SS</sub>  | CKE0_B           | CKE1_B           |   |   | CK_t_B           | CK_c_B           | V <sub>SS</sub>  | CA5_B           | V <sub>SS</sub>  |
| R  | V <sub>DD2</sub> | CA0_B           | CS1_B            | CS0_B            | V <sub>DD2</sub> |   |   | V <sub>DD2</sub> | CA2_B            | CA3_B            | CA4_B           | V <sub>DD2</sub> |
| T  | V <sub>SS</sub>  | ODT_CA_B        | V <sub>SS</sub>  | V <sub>DD1</sub> | V <sub>SS</sub>  |   |   | V <sub>SS</sub>  | V <sub>DD1</sub> | V <sub>SS</sub>  | RESET_n         | V <sub>SS</sub>  |
| U  | V <sub>DD1</sub> | DQ3_B           | V <sub>DDQ</sub> | DQ4_B            | V <sub>DD2</sub> |   |   | V <sub>DD2</sub> | DQ12_B           | V <sub>DDQ</sub> | DQ11_B          | V <sub>DD1</sub> |
| V  | V <sub>SS</sub>  | DQ2_B           | DQS0_c_B         | DQ5_B            | V <sub>SS</sub>  |   |   | V <sub>SS</sub>  | DQ13_B           | DQS1_c_B         | DQ10_B          | V <sub>SS</sub>  |
| W  | V <sub>DDQ</sub> | V <sub>SS</sub> | DQS0_t_B         | V <sub>SS</sub>  | V <sub>DDQ</sub> |   |   | V <sub>DDQ</sub> | V <sub>SS</sub>  | DQS1_t_B         | V <sub>SS</sub> | V <sub>DDQ</sub> |
| Y  | V <sub>SS</sub>  | DQ1_B           | DMI0_B           | DQ6_B            | V <sub>SS</sub>  |   |   | V <sub>SS</sub>  | DQ14_B           | DMI1_B           | DQ9_B           | V <sub>SS</sub>  |
| AA | DNU              | DQ0_B           | V <sub>DDQ</sub> | DQ7_B            | V <sub>DDQ</sub> |   |   | V <sub>DDQ</sub> | DQ15_B           | V <sub>DDQ</sub> | DQ8_B           | DNU              |
| AB | DNU              | DNU             | V <sub>SS</sub>  | V <sub>DD2</sub> | V <sub>SS</sub>  |   |   | V <sub>SS</sub>  | V <sub>DD2</sub> | V <sub>SS</sub>  | DNU             | DNU              |
|    | 1                | 2               | 3                | 4                | 5                | 6 | 7 | 8                | 9                | 10               | 11              | 12               |

Top View (ball down)

 LPDDR4\_A(Channel A)  LPDDR4\_B(Channel B)  ZQ,ODT\_CA,RESET  Supply  Ground



## 2.3. Pad Definition

| Symbol                                                       | Type  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|--------------------------------------------------------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CK_t_A, CK_c_A<br>CK_t_B, CK_c_B                             | Input | <b>Clock:</b> CK_t and CK_c are differential clock inputs. All address, command and control input signals are sampled on positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to clock. Each channel (A, B) has its own clock pair.                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| CKE0_A, CK1_A<br>CKE0_B, CK1_B                               | Input | <b>Clock enable:</b> CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is sampled at the rising edge of CK.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| CS0_A, CS1_A<br>CS0_B, CS1_B                                 | Input | <b>Chip select:</b> Each channel (A, B) has its own CS signals.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| CA[5:0]_A<br>CA[5:0]_B                                       | Input | <b>Command/address inputs:</b> Provide the command and address inputs according to the command truth table. Each channel (A, B) has its own CA signals.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| ODT_CA_A<br>ODT_CA_B                                         | Input | <b>LPDDR4 CA ODT control:</b> The ODT_CA pin is used in conjunction with the mode register to turn on/off the on-die termination for CA pins. It is bonded to VDD2 within the package, or at the package ball, for the terminating rank, and the non-terminating ranks are bonded to VSS (or left floating with a weak pull-down on the DRAM die). The terminating rank is the DRAM that terminates the CA bus for all die on the same channel.<br><b>LPDDR4X CA ODT Control:</b> The ODT_CA pin is ignored by LPDDR4X devices. CA ODT is fully controlled through MR11 and MR22. The ODT_CA pin shall be connected to a valid logic level.                                                                                 |
| DQ[15:0]_A<br>DQ[15:0]_B                                     | I/O   | <b>Data input/output:</b> Bidirectional data bus.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| DQS[1:0]_t_A<br>DQS[1:0]_c_A<br>DQS[1:0]_t_B<br>DQS[1:0]_c_B | I/O   | <b>Data strobe:</b> DQS_t and DQS_c are bidirectional differential output clock signals used to strobe data during a READ or WRITE. The data strobe is generated by the DRAM for a READ and is edge-aligned with data. The data strobe is generated by the SoC memory controller for a WRITE and is trained to precede data. Each byte of data has a data strobe signal pair. Each channel (A, B) has its own DQS_t and DQS_c strobes.                                                                                                                                                                                                                                                                                      |
| DMI[1:0]_A<br>DMI[1:0]_B                                     | I/O   | <b>Data mask/Data bus inversion:</b> DMI is a dual use bidirectional signal used to indicate data to be masked, and data which is inverted on the bus. For data bus inversion (DBI), the DMI signal is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. DBI can be disabled via a mode register setting. For data mask, the DMI signal is used in combination with the data lines to indicate data to be masked in a MASK WRITE command (see the Data Mask (DM) and Data Bus Inversion (DBI) sections for details). The data mask function can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel has its own DMI signals. |



## Pad Definition (continue)

| Symbol                            | Type      | Description                                                                                                                                                                                     |
|-----------------------------------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ZQ0, ZQ1                          | Reference | <b>ZQ calibration reference:</b> Used to calibrate the output drive strength and the termination resistance. The ZQ pin shall be connected to $V_{DDQ}$ through a $240\Omega \pm 1\%$ resistor. |
| $V_{DDQ}$ , $V_{DD1}$ , $V_{DD2}$ | Supply    | <b>Power supplies:</b> Isolated on the die for improved noise immunity.                                                                                                                         |
| $V_{SS}$                          | Supply    | <b>Ground reference:</b> Power supply ground reference.                                                                                                                                         |
| RESET_n                           | Input     | <b>RESET:</b> When asserted LOW, the RESET pin resets all channels of the die.                                                                                                                  |
| DNU                               | –         | <b>Do not use:</b> Must be grounded or left floating.                                                                                                                                           |
| NC                                | –         | <b>No connect:</b> Not internally connected.                                                                                                                                                    |

*Notes : LPDDR4X pad definitions are the same as LPDDR4, except ODT\_CA pins as described in the Table.*

**10mm \* 14.5mm \* 1.10mm Max (Package Code: D)**

200X  $\varnothing 0.363 \pm 0.05$

$\varnothing 0.15$  (M) A B C  
 $\varnothing 0.05$  (M) A

4

14.5

13.65 CTR

0.65 TYP

0.8 TYP

8.8 CTR

10

B

C

12 11 10 9 8 5 4 3 2 1

A B C D E F G H J K L M N P R T U V W Y AA AB

PIN A1 INDEX

0.1

0.227  $\pm$  0.05

(1.10 MAX)

6

3

2

5

5 MAX

4.4 MAX

0.9 MAX

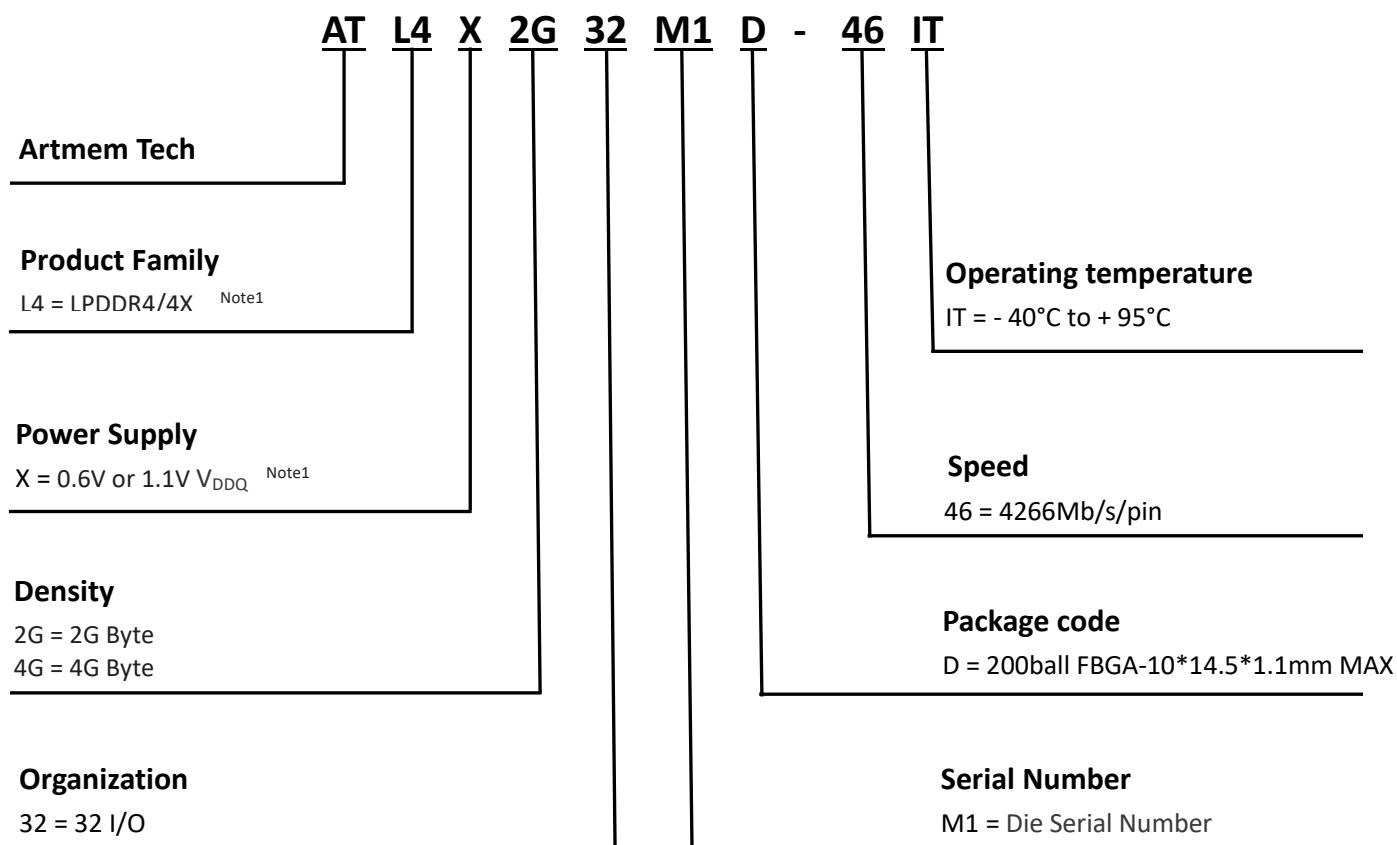
1.5 MAX

3.



## Core Specifications

### 3.1. Part Number Decoding



**Note1:** LPDDR4X :  $V_{DD1} = 1.80V$ ;  $V_{DD2} = 1.10V$ ;  $V_{DDQ} = 0.60V$ ;  
LPDDR4:  $V_{DD1} = 1.80V$ ;  $V_{DD2} = 1.10V$ ;  $V_{DDQ} = 1.10V$ ;



## 3.2. Ordering Options

Table 1: Key Timing Parameters

| Speed Grade | Clock Rate (MHz) | Data Rate (Mb/s/pin) | WRITE Latency |       | READ Latency |             |
|-------------|------------------|----------------------|---------------|-------|--------------|-------------|
|             |                  |                      | Set A         | Set B | DBI Disabled | DBI Enabled |
| -46         | 2133             | 4266                 | 18            | 34    | 36           | 40          |

Table 2: Part Number List

| Part Number       | Total Density | Data Rate     | Operating temperature |
|-------------------|---------------|---------------|-----------------------|
| ATL4X2G32M1D-46IT | 2GB(16Gb)     | 4266 Mb/s/pin | -40°C to + 95°C       |
| ATL4X4G32M1D-46IT | 4GB(32Gb)     | 4266 Mb/s/pin | -40°C to + 95°C       |

Table 3: Refresh Requirement Parameters

| Parameter                                                  | Symbol        | 8Gb Per Channel | unit |
|------------------------------------------------------------|---------------|-----------------|------|
| REFRESH cycle time (all banks)                             | $t_{RFCab}$   | 280             | ns   |
| REFRESH cycle time (per bank)                              | $t_{RFCpb}$   | 140             | ns   |
| Per bank refresh to per bank refresh time (different bank) | $t_{PBR2PBR}$ | 90              | ns   |

**Notes :** This table only describes refresh parameters which are density dependent. Refer to Refresh Requirement section in General LPDDR4X specification for all the refresh parameters.



### 3.3. Die Addressing Table

| Configuration                       |                                         | 2G32<br>(16Gb/package)                | 4G32<br>(32Gb/package)                |
|-------------------------------------|-----------------------------------------|---------------------------------------|---------------------------------------|
| Die Configuration<br>in the package | Channel A, rank 0                       | x16 mode × 1 die<br>(dual channel)    | x16 mode × 1 die<br>(dual channel)    |
|                                     | Channel B, rank 0                       |                                       |                                       |
|                                     | Channel A, rank 1                       | -                                     | x16 mode × 1 die<br>(dual channel)    |
|                                     | Channel B, rank 1                       |                                       |                                       |
| Die Addressing                      | Memory density (per die)                | 16Gb                                  | 16Gb                                  |
|                                     | Memory density (per channel)            | 8Gb                                   | 8Gb                                   |
|                                     | Configuration                           | 64Mb × 16 DQ ×<br>8 banks × 2channels | 64Mb × 16 DQ ×<br>8 banks × 2channels |
|                                     | Number of channels (per die)            | 2                                     | 2                                     |
|                                     | Number of banks (per channel)           | 8                                     | 8                                     |
|                                     | Array prefetch (bits, per channel)      | 256                                   | 256                                   |
|                                     | Number of rows (per channel)            | 65,336                                | 65,336                                |
|                                     | Number of columns<br>(fetch boundaries) | 64                                    | 64                                    |
|                                     | Page size (bytes)                       | 2048                                  | 2048                                  |
|                                     | Channel density (bits per channel)      | 8,589,934,592                         | 8,589,934,592                         |
|                                     | Total density (bits per die)            | 17,179,869,184                        | 17,179,869,184                        |
|                                     | Bank address                            | BA[2:0]                               | BA[2:0]                               |
|                                     | Row address                             | R[15:0]                               | R[15:0]                               |
|                                     | Column address                          | C[9:0]                                | C[9:0]                                |
|                                     | Burst starting address boundary         | 64-bit                                | 64-bit                                |

**Notes :** Refer to Package Block Diagrams section in Product specification  
and SDRAM Addressing Section in General LPDDR4X specification.



### 3.4. Mode Register Contents

| MR0 |                   |                                                                                                                                                                                                                |
|-----|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| OP7 |                   | <b>OP[0] = 1b:</b> Only modified refresh mode supported<br><b>OP[1] = 0b:</b> Device supports normal latency<br><b>OP[2] = 0b:</b> Device supports TRR<br><b>OP[5] = 1b:</b> Device supports single-ended mode |
| OP6 |                   |                                                                                                                                                                                                                |
| OP5 | Single-ended mode |                                                                                                                                                                                                                |
| OP4 |                   |                                                                                                                                                                                                                |
| OP3 |                   |                                                                                                                                                                                                                |
| OP2 | RFM support       |                                                                                                                                                                                                                |
| OP1 | Latency Mode      |                                                                                                                                                                                                                |
| OP0 | REF               |                                                                                                                                                                                                                |
|     |                   |                                                                                                                                                                                                                |
| MR5 |                   |                                                                                                                                                                                                                |
| OP7 | Manufacturer ID   | 1111 1111b : Micron                                                                                                                                                                                            |
| OP6 |                   |                                                                                                                                                                                                                |
| OP5 |                   |                                                                                                                                                                                                                |
| OP4 |                   |                                                                                                                                                                                                                |
| OP3 |                   |                                                                                                                                                                                                                |
| OP2 |                   |                                                                                                                                                                                                                |
| OP1 |                   |                                                                                                                                                                                                                |
| OP0 |                   |                                                                                                                                                                                                                |
|     |                   |                                                                                                                                                                                                                |
| MR8 |                   |                                                                                                                                                                                                                |
| OP7 | I/O width         | <b>OP[7:6] = 00b:</b> x16/channel                                                                                                                                                                              |
| OP6 |                   |                                                                                                                                                                                                                |
| OP5 | Density           | <b>OP[5:2] = 0100b:</b> 16Gb dual-channel die                                                                                                                                                                  |
| OP4 |                   |                                                                                                                                                                                                                |
| OP3 |                   |                                                                                                                                                                                                                |
| OP2 |                   |                                                                                                                                                                                                                |
| OP1 |                   |                                                                                                                                                                                                                |
| OP0 |                   |                                                                                                                                                                                                                |

| MR3  |                   |                                                                                                                                               |
|------|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| OP7  |                   | <b>OP[2]= 0b:</b> PPR protection disabled (default)<br><b>1b:</b> PPR protection enabled                                                      |
| OP6  |                   |                                                                                                                                               |
| OP5  |                   |                                                                                                                                               |
| OP4  |                   |                                                                                                                                               |
| OP3  |                   |                                                                                                                                               |
| OP2  | PPRP <sup>3</sup> |                                                                                                                                               |
| OP1  |                   |                                                                                                                                               |
| OP0  |                   |                                                                                                                                               |
|      |                   |                                                                                                                                               |
| MR6  |                   |                                                                                                                                               |
| OP7  | Revision ID1      | 0000 0111b                                                                                                                                    |
| OP6  |                   |                                                                                                                                               |
| OP5  |                   |                                                                                                                                               |
| OP4  |                   |                                                                                                                                               |
| OP3  |                   |                                                                                                                                               |
| OP2  |                   |                                                                                                                                               |
| OP1  |                   |                                                                                                                                               |
| OP0  |                   |                                                                                                                                               |
|      |                   |                                                                                                                                               |
| MR13 |                   |                                                                                                                                               |
| OP7  |                   | <b>OP[2]= 0b:</b> Normal operation (default)<br><b>1b:</b> Output the V <sub>REF(CA)</sub> value on DQ7 and V <sub>REF(DQ)</sub> value on DQ6 |
| OP6  |                   |                                                                                                                                               |
| OP5  |                   |                                                                                                                                               |
| OP4  |                   |                                                                                                                                               |
| OP3  |                   |                                                                                                                                               |
| OP2  | VR0               |                                                                                                                                               |
| OP1  |                   |                                                                                                                                               |
| OP0  |                   |                                                                                                                                               |



## Mode Register Contents (continue)

| MR24 |               |                                                                                                                          |
|------|---------------|--------------------------------------------------------------------------------------------------------------------------|
| OP7  | TRR Mode      | <b>OP[3:0] =</b><br><b>1000b:</b> Unlimited MAC<br><b>OP[7] =</b><br><b>0b:</b> Disable (default)<br><b>1b:</b> Reserved |
| OP6  |               |                                                                                                                          |
| OP5  |               |                                                                                                                          |
| OP4  |               |                                                                                                                          |
| OP3  | Unlimited MAC |                                                                                                                          |
| OP2  | MAC Value     |                                                                                                                          |
| OP1  |               |                                                                                                                          |
| OP0  |               |                                                                                                                          |

| MR25 |                            |        |                                                                                        |
|------|----------------------------|--------|----------------------------------------------------------------------------------------|
| OP7  | PPR resources <sup>4</sup> | Bank 7 | <b>0b:</b><br>PPR resource is not available<br><b>1b:</b><br>PPR resource is available |
| OP6  |                            | Bank 6 |                                                                                        |
| OP5  |                            | Bank 5 |                                                                                        |
| OP4  |                            | Bank 4 |                                                                                        |
| OP3  |                            | Bank 3 |                                                                                        |
| OP2  |                            | Bank 2 |                                                                                        |
| OP1  |                            | Bank 1 |                                                                                        |
| OP0  |                            | Bank 0 |                                                                                        |

- Notes:**
1. The contents of Product Specific Mode Register definition will reflect information specific to each die in these package
  2. Other bits not defined above and other mode registers are referred to in Mode Register Assignments and Definitions section.
  3. When not using PPR function, PPR protection should be enabled to prevent unintended PPR entry (MR3 OP[2] = 1b).
  4. Before using PPR function, confirm the availability of PPR resource by reading MR25.